GSV6127E

Type-C/DisplayPort 1.4/HDMI 2.0 to MIPI/LVDS Converter with Audio Extraction and Embedded MCU

May, 2024

Product Specification

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Glossary

DDC	Display Data Channel
EDID	Extended Display Identification Data
ESD	Electrostatic Discharge
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detect
I²C	Inter-Integrated Circuit
MCU	Microcontroller Unit
MISO	Master In Slave Out
MOSI	Master Out Slave In
OTP	One Time Programmable
PCM	Pulse Code Modulation
S/PDIF	Sony/Philips Digital Interface Format
SPI	Serial Peripheral Interface
TMDS	Transition Minimized Differential Signaling
SCDC	Status and Control Data Channel
CEC	Consumer Electronics Control
AUX	AUX_CH, DisplayPort Auxiliary Channel
DPCD	DisplayPort Configuration Data
Main-Link	Unidirectional channel stream from DPTX to DPRX
SDP	Secondary-data Packet
DDC/CI	VESA Display Data Channel/Command Interface
MCCS	Monitor Control Command Set (VESA)
DP	DisplayPort (VESA)
DPRX	DisplayPort Receiver
DPTX	DisplayPort Transmitter
DSC	Display Stream Compression
FEC	Forward Error Correction
HBR	DisplayPort High Bit Rate, HDMI High Bit-Rate Audio
MST	DisplayPort Multi-Stream Transport
SSC	Spread-Spectrum Clock

1. General Description

1.1 General Information

Gscoolink GSV6127E is a high-performance, low-power Type-C/DisplayPort 1.4/HDMI 2.0 to MIPI CSI-2/LVDS converter. With Dual Port MIPI interface, genuine 4K60 444 can be transmitted using MIPI interface. By integrating enhanced microcontroller, GSV6127E has created a cost-effective solution that provides time-to-market advantages. The DisplayPort Receiver supports up to 32.4Gbps (HBR3, 4-lane), the HDMI Receiver supports up to 18Gbps (TMDS, 6G/3-lane). With embedded Channel Configuration (CC), Power Delivery (PD) controller and Billboard USB 2.0 controller, GSV6127E can support Type-C Alternate DisplayPort/HDMI to MIPI/Audio Extraction application. The superior architecture of GSV6127E provides economical smaller footprint solutions using QFN76, targeting automotive and video conference applications.

HDCP 1.4 and HDCP 2.2/2.3 are implemented in GSV6127E for its DisplayPort/HDMI Rx port. Color Space Conversion, 420-444/422 Conversion, De-Interlacer and Downscaler are supported for flexible video processing. Audio Extraction of DisplayPort/HDMI Rx is supported in GSV6127E for audio processing. With audio sample raw data detection feature, LPCM channel filled with consistent zero raw sample data will be automatically detected and muted.

Within 8kV HBM tolerance for Type-C interface pins, GSV6127E's operation temperature range is -40 ºC to 85 ºC using automotive qualified process.

An internal Video Generator can be used to generate any uncompressed video timing defined in DisplayPort HBR3 bandwidth, such as 4K@60Hz, 4K@30Hz, 480i@60Hz.

With embedded MCU and PD 3.0 controller, GSV6127E can be used with customized with external PMIC to charge external devices as source using Type-C interface.

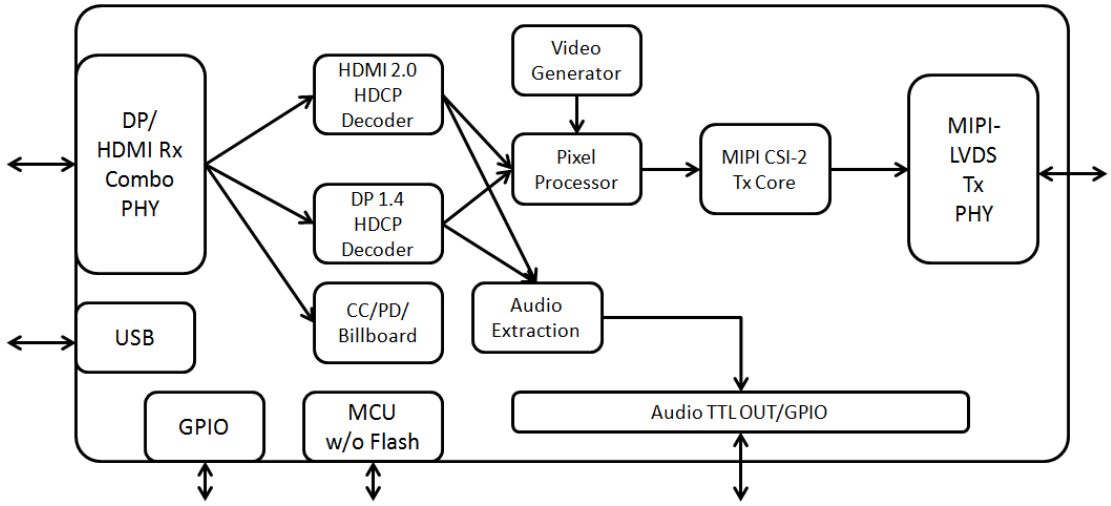


Figure 1. Top Diagram

The supported audio formats are listed in Table 1.

Table 1. Supported Audio Format

Packet ID	Packet Type	Sampling Frequency (KHz)		
		32/44.1/48/88.2/ 96/176.4/192	256/352.8/384/ 512/705.6/768	64/128
0x02	Audio Sample Packet (LPCM and Compressed Audio)	Y		Y
0x07	One Bit Audio Sample Packet	Y		
0x08	DST Audio Packet	Y		
0x09	High Bit-rate Audio Stream Packet	Y	Y	

1.2 Features

1.2.1 DisplayPort Receiver

- Compliant with VESA DisplayPort 1.4a
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Compliant with both DisplayPort and USB Type-C Alternative Mode
- Support HBR3, HBR2, HBR and RBR (8.1/5.4/2.7/1.62 Gbps)
- Flexible 1/2/4 lane Main-Link configuration
- Programmable Adaptive Equalization
- Support Full-Link Training and No-Link Training
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Audio Extraction
- Support Horizontal Blanking Expansion up to 4K@60Hz format
- Embedded arbitrary EDID and MCCS

- Support Spread Spectrum Clock (SSC)
- 3D format support of frame sequential, stacked frame, side-by-side, top-to-bottom

1.2.2 HDMI Receiver

- Compliant with HDMI 2.0b, HDMI 1.4b
- Compliant with HDCP 2.2/2.3 and HDCP 1.4 in repeater/receiver mode
- Data rate up to 18Gbps (TMDS 6Gbps/3 Lane)
- Programmable Adaptive Equalization
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Embedded arbitrary EDID (up to 512 bytes)
- 5V tolerance on DDC/HPD pins
- 3D format support of frame packing, side-by-side, top-and-bottom

1.2.3 MIPI CSI-2 Transmitter

- Support MIPI CSI-2 v3.0 version transmission using D-PHY interface
- Support 2.5G bps 1/2/3/4/8-lane MIPI D-PHY Out
- Programmable output swing , slew-rate and pre-emphasis
- CSI-2 Lane Reassignment and Polarity Flip
- Support RGB888, RGB666, RGB565, RGB555, RGB444
- Support YUV 4:2:2 8-bit, 10-bit, 12-bit
- Support YUV 4:2:0 legacy 8-bit
- Support burst and non-burst mode

1.2.4 Dual-Port LVDS Transmitter

- Compatible with VESA and JEIDA standards
  - Single/Dual-Port LVDS Transmitter
  - Programmable output swing , slew-rate , common voltage and pre-emphasis
  - Data rate up to 1.5Gbps per lane

1.2.5 USB Type-C DisplayPort Alternative Mode Receiver

- Compliant with USB Type-C 1.1/1.0 Specification
- Compliant with USB Power Delivery 3.0 Specification
- Programmable USB Type-C Channel Configuration function

- Support Billboard in USB 2.0

1.2.6 Pixel Processor

- Color Space conversion
- YCbCr 444/422-420 timing conversion
- Downscaler with fixed horizontal and vertical 2 ratio for 4K to 2K conversion
- Deinterlacer for interlaced timing

1.2.7 Audio Output

- I2S and SPDIF Audio Extraction from DisplayPort Rx /Type-C Rx
- SPDIF/I2S/HBR/DSD/TDM Format Supported for Audio Extraction

1.2.8 System Features

- Optional External MCU (via I2C)/ Internal MCU mode
- Embedded MCU using External Flash
- External 25MHz Crystal required
- Available Pins for UART/Timer/GPIO control from embedded MCU
- Mailbox feature for external MCU access on chip function status
- Temperature Sensor Monitoring Circuit

1.3 Chip Application Modes

1.3.1 Type-C Alt-Mode In to MIPI Out Application

RxPort is configured as Type-C Alt-Mode (DisplayPort) Rx Input. Together with on-chip CC, USB 2.0 support, Type-C USB input can be configured to DisplayPort 1.4a input stream for processing. This mode is designed for Type-C to SoC MIPI panel front-end interconnection. If required, the MIPI interface can also be set to LVDS for output (up to 4K30 timing). MIPI D-PHY interface interconnection are both applicable based on application designs.

With internal Color Space Converter, De-Interlacer and Downscaler, DisplayPort input timing can be converted to MIPI compatible output timing. With Downscaler in Pixel Processor, output can be downscaled automatically when video stream bandwidth exceeds downstream capability.

Meanwhile, Audio extraction can be applicable if required.

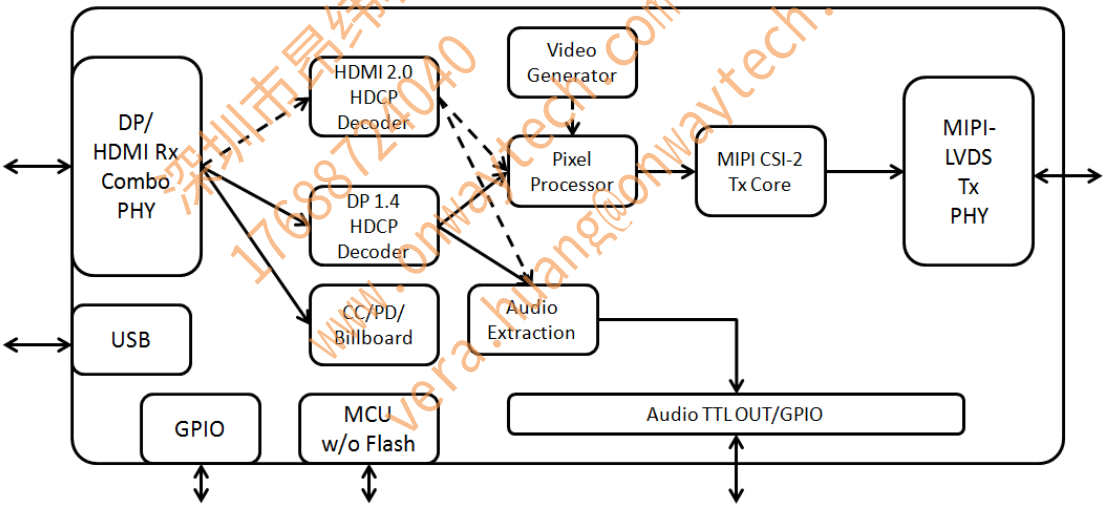


Figure 2. Type-C Alt-Mode In to MIPI Out Application

In order to control external PMIC, extra MIPI-B or AUD1/AUD2 bus can be reused as GPIO for further control. PMIC, Vconn, Vbus can thus be controlled. I2S/SPDIF Extraction and TDM Extraction Pin assignment examples are shown below.

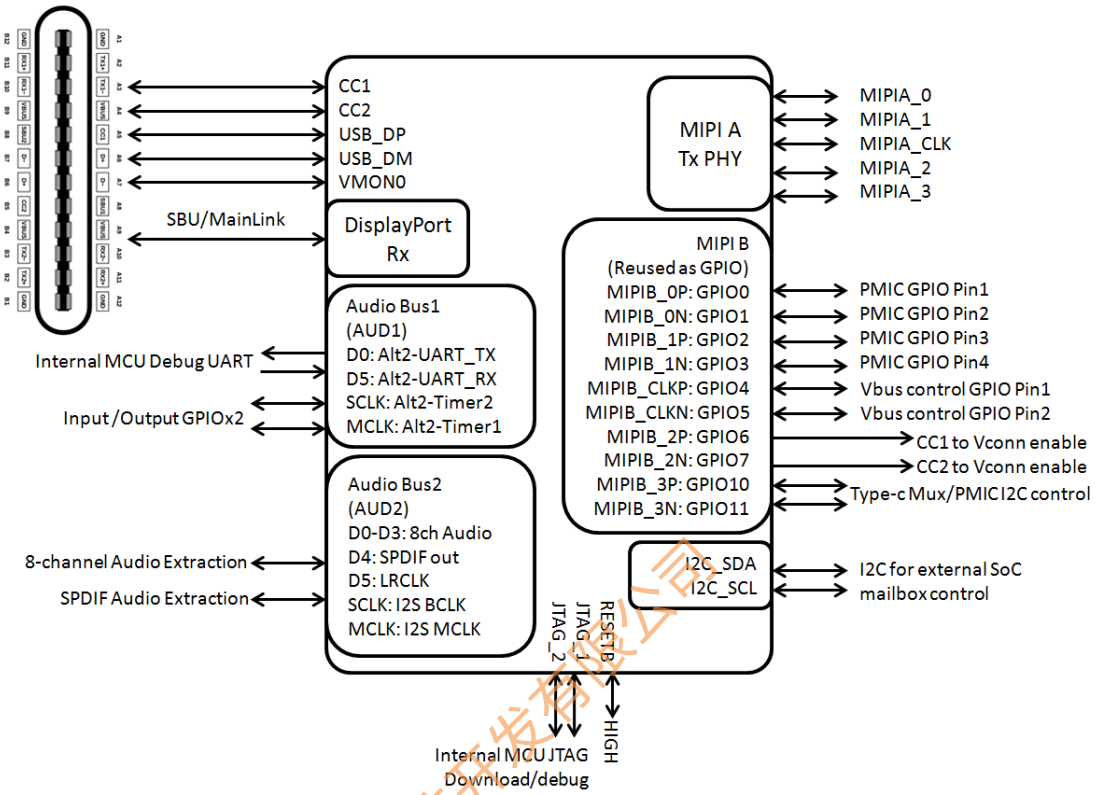


Figure 3. Type-C Alt-Mode Mode I2S/SPDIF Extraction Pin Assignment Example

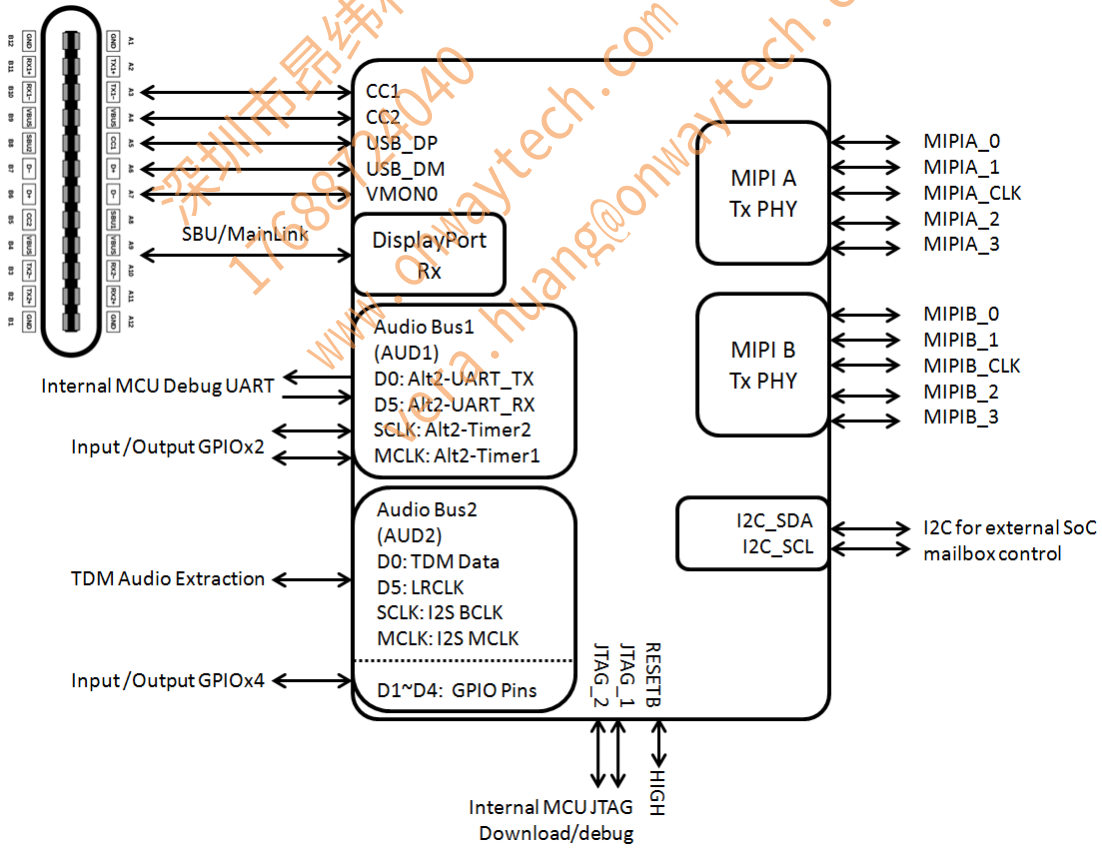


Figure 4. Type-C Alt-Mode Mode TDM Extraction Pin Assignment Example

1.3.2 HDMI In to MIPI Out Application

RxPort is configured as HDMI 2.0 Input. This mode is designed for HDMI 2.0 to SoC MIPI panel front-end interconnection. If required, the MIPI interface can also be set to LVDS for output (up to 4K60 420 timing).

With internal Color Space Converter, De-Interlacer, HDMI 2.0 input timing can be converted to MIPI compatible output timing. With Downscaler in Pixel Processor, output can be downscaled automatically when video stream bandwidth exceeds downstream capability.

Meanwhile, Audio extraction can be applicable if required.

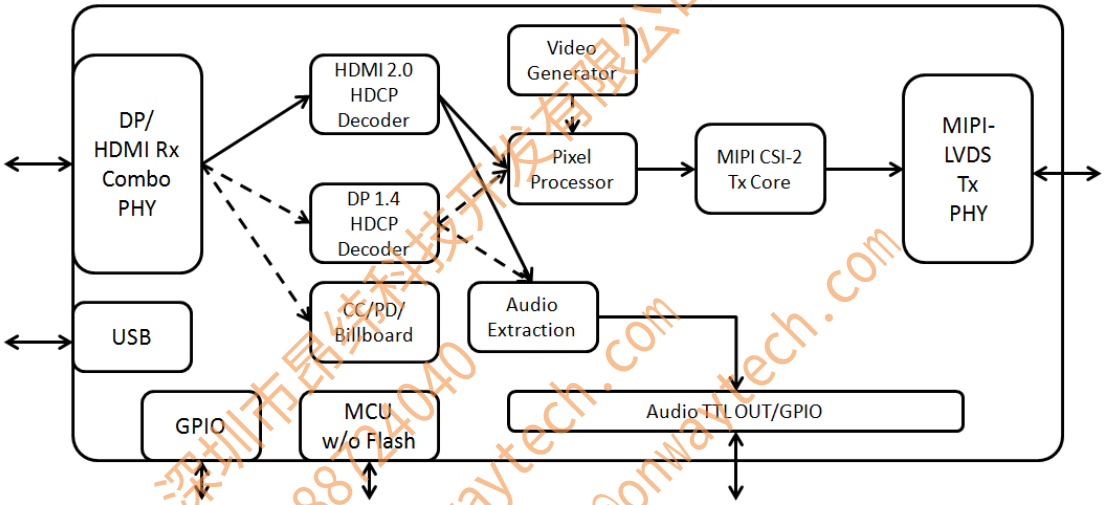


Figure 5. HDMI In to MIPI Out Application

1.4 Audio Bus Output Configuration

When one group of audio bus is configured as output, I2S and SPDIF are output at the same time. General configuration of pin settings is shown below:

Table 2. I2S/SPDIF Audio Extraction

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Output	I2S Data, default stereo channels
AUD_D1	SDATA[1]	Output	I2S Data, 3/4 channels
AUD_D2	SDATA[2]	Output	I2S Data, 5/6 channels
AUD_D3	SDATA[3]	Output	I2S Data, 7/8 channels
AUD_D4	SPDIF	Output	SPDIF channel

AUD_D5	LRCLK/WS	Output	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Output	Fixed to 64Fs
MCLK	Sys Clock	Output	Selected from 128Fs/256Fs/384Fs/512Fs

For HBR application, SPDIF is also capable of sending out with 4 pins.

Table 3. HBR Audio Extraction in SPDIF

Pin Name	Alias	Direction	Description
AUD_D0	SPDIF[0]	Output	SPDIF Data[0], 1/2 channels
AUD_D1	SPDIF[1]	Output	SPDIF Data[1], 3/4 channels
AUD_D2	SPDIF[2]	Output	SPDIF Data[2], 5/6 channels
AUD_D3	SPDIF[3]	Output	SPDIF Data[3], 7/8 channels
AUD_D4	SPDIF	Output	SPDIF channel, 1/2 channels

For TDM format, a fixed format of TDM-8 can be enabled. The Format is listed as below.

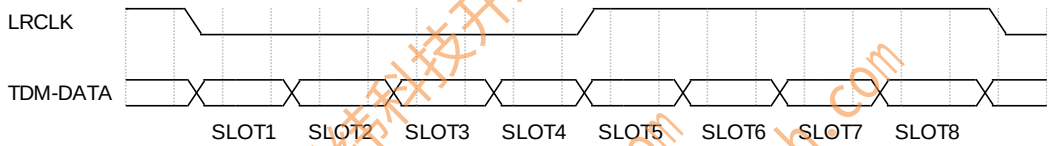


Figure 6. TDM-8 Format

Table 4. TDM Audio Extraction Format

Slot Name	LPCM 2.0 Audio	LPCM 5.1 Audio	LPCM 7.1 Audio
SLOT1	Stereo L	5.1-L	7.1-L
SLOT2	Stereo R	5.1-R	7.1-R
SLOT3		5.1-C	7.1-C
SLOT4		5.1-LFE	7.1-LFE
SLOT5		5.1-LS	7.1-LS
SLOT6		5.1-RS	7.1-RS
SLOT7			7.1-LRS
SLOT8			7.1-RRS

2. Pin Description

2.1 Pin Diagram

QFN76 Pin definition is defined as below.

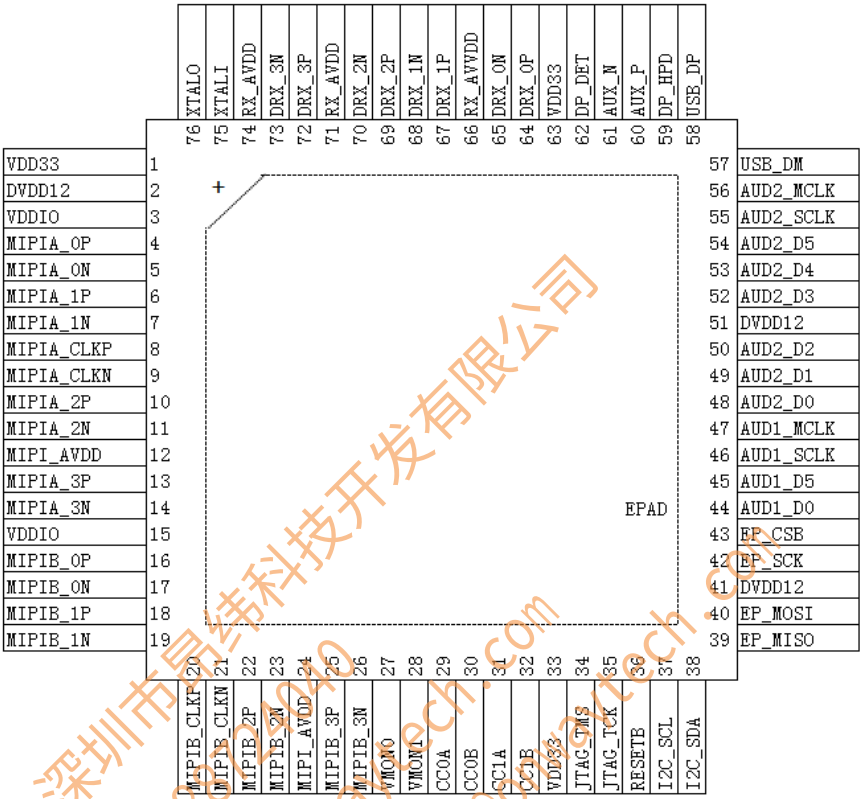


Figure 7. GSV6127E QFN76 Pin Diagram

2.2 QFN76 Pin Description

Table 5. QFN76 Pin Description

Pin Name	Direction	Pin No.	Description
DisplayPort RX Pins			
DP_DET	I	62	HDMI: RX 5V Detection PAD DP: RX DP Detection PAD
DP_HPD	O	59	HDMI: RX HPD PAD DP: RX HPD PAD
AUX_P	I/O	60	HDMI: RX DDC SDA PAD DP: RX AUX_P PAD
AUX_N	I/O	61	HDMI: RX DDC SCL PAD DP: RX AUX_N PAD

DRX_0N	I	65	HDMI: RX Positive TMDS clock differential input DP: RX Negative Main-Link differential data input [0]
DRX_0P	I	64	HDMI: RX Negative TMDS clock differential input DP: RX Positive Main-Link differential data input [0]
DRX_1N	I	68	HDMI: RX Positive TMDS differential data input [0] DP: RX Negative Main-Link differential data input [1]
DRX_1P	I	67	HDMI: RX Negative TMDS differential data input [0] DP: RX Positive Main-Link differential data input [1]
DRX_2N	I	70	HDMI: RX Positive TMDS differential data input [1] DP: RX Negative Main-Link differential data input [2]
DRX_2P	I	69	HDMI: RX Negative TMDS differential data input [1] DP: RX Positive Main-Link differential data input [2]
DRX_3N	I	73	HDMI: RX Positive TMDS differential data input [2] DP: RX Negative Main-Link differential data input [3]
DRX_3P	I	72	HDMI: RX Negative TMDS differential data input [2] DP: RX Positive Main-Link differential data input [3]
Power/Ground Pins			
DVDD12	Power	2,41,51,	Digital 1.2V voltage power supply
VDDIO	Power	3,15,	Digital IO 3.3V voltage power supply
VDD33	Power	33,63,	Analog/Digital 3.3V voltage power supply
TVDD	Power	1,	Analog 3.3V voltage power supply for RX Port
RX_AVDD	Power	66,71,74	Analog 1.2V voltage power supply for RX Port
DPHY_AVDD	Power	12,24,	Analog 1.2V voltage power supply for Parallel Port
MIPI Tx Pins			
MIPIA_0P	O	4	MIPI: PORTA D-PHY Data[0] differential positive output LVDS: Video In/Out, Positive LVDS Data[0] VESA: PORTA Positive LVDS Data[0] Alternate: Digital IO PAD as GPIO0
MIPIA_0N	O	5	MIPI: PORTA D-PHY Data[0] differential negative output LVDS: Video In/Out, Negative LVDS Data[0] VESA: PORTA Negative LVDS Data[0] Alternate: Digital IO PAD as GPIO1
MIPIA_1P	O	6	MIPI: PORTA D-PHY Data[1] differential positive output LVDS: Video In/Out, Positive LVDS Data[1] VESA: PORTA Positive LVDS Data[1] Alternate: Digital IO PAD as GPIO2

MIPIA_1N	O	7	MIPI: PORTA D-PHY Data[1] differential negative output LVDS: Video In/Out, Negative LVDS Data[1] VESA: PORTA Negative LVDS Data[1] Alternate: Digital IO PAD as GPIO3
MIPIA_CLKP	O	8	MIPI: PORTA D-PHY clock differential positive output LVDS: Video In/Out, Positive LVDS Data[2] VESA: PORTA Positive LVDS Clock Alternate: Digital IO PAD as GPIO4
MIPIA_CLKN	O	9	MIPI: PORTA D-PHY clock differential negative output LVDS: Video In/Out, Negative LVDS Data[2] VESA: PORTA Negative LVDS Clock Alternate: Digital IO PAD as GPIO5
MIPIA_2P	O	10	MIPI: PORTA D-PHY Data[2] differential positive output LVDS: Video In/Out, Positive LVDS Data[3] VESA: PORTA Positive LVDS Data[2] Alternate: Digital IO PAD as GPIO6
MIPIA_2N	O	11	MIPI: PORTA D-PHY Data[2] differential negative output LVDS: Video In/Out, Negative LVDS Data[3] VESA: PORTA Negative LVDS Data[2] Alternate: Digital IO PAD as GPIO7
MIPIA_3P	O	13	MIPI: PORTA D-PHY Data[3] differential positive output LVDS: Video In/Out, Positive LVDS Data[4] VESA: PORTA Positive LVDS Data[3] Alternate: Digital IO PAD as GPIO10
MIPIA_3N	O	14	MIPI: PORTA D-PHY Data[3] differential negative output LVDS: Video In/Out, Negative LVDS Data[4] VESA: PORTA Negative LVDS Data[3] Alternate: Digital IO PAD as GPIO11
MIPIB_0P	O	16	MIPI: PORTB D-PHY Data[0] differential positive output LVDS: Video In/Out, Positive LVDS Data[7] VESA: PORTB Positive LVDS Data[0] Alternate: Digital IO PAD as GPIO0
MIPIB_0N	O	17	MIPI: PORTB D-PHY Data[0] differential negative output LVDS: Video In/Out, Negative LVDS Data[7] VESA: PORTB Negative LVDS Data[0] Alternate: Digital IO PAD as GPIO1

MIPIB_1P	O	18	MIPI: PORTB D-PHY Data[1] differential positive output LVDS: Video In/Out, Positive LVDS Data[8] VESA: PORTB Positive LVDS Data[1] Alternate: Digital IO PAD as GPIO2
MIPIB_1N	O	19	MIPI: PORTB D-PHY Data[1] differential negative output LVDS: Video In/Out, Negative LVDS Data[8] VESA: PORTB Negative LVDS Data[1] Alternate: Digital IO PAD as GPIO3
MIPIB_CLKP	O	20	MIPI: PORTB D-PHY clock differential positive output LVDS: Video In/Out, Positive LVDS Data[9] VESA: PORTB Positive LVDS Clock Alternate: Digital IO PAD as GPIO4
MIPIB_CLKN	O	21	MIPI: PORTB D-PHY clock differential negative output LVDS: Video In/Out, Negative LVDS Data[9] VESA: PORTB Negative LVDS Clock Alternate: Digital IO PAD as GPIO5
MIPIB_2P	O	22	MIPI: PORTB D-PHY Data[2] differential positive output LVDS: Video In/Out, Positive LVDS Data[10] VESA: PORTB Positive LVDS Data[2] Alternate: Digital IO PAD as GPIO6
MIPIB_2N	O	23	MIPI: PORTB D-PHY Data[2] differential negative output LVDS: Video In/Out, Negative LVDS Data[10] VESA: PORTB Negative LVDS Data[2] Alternate: Digital IO PAD as GPIO7
MIPIB_3P	O	25	MIPI: PORTB D-PHY Data[3] differential positive output LVDS: Video In/Out, Positive LVDS Data[11] VESA: PORTB Positive LVDS Data[3] Alternate: Digital IO PAD as GPIO10
MIPIB_3N	O	26	MIPI: PORTB D-PHY Data[3] differential negative output LVDS: Video In/Out, Negative LVDS Data[11] VESA: PORTB Negative LVDS Data[3] Alternate: Digital IO PAD as GPIO11
Digital pins			
I2C_SDA	I/O	38	Default: Digital IO for I2C Data Alternate: GPIO8 for internal MCU
I2C_SCL	I/O	37	Default: Digital IO for I2C Clock Alternate: GPIO9 for internal MCU

AUD1_SCLK	I/O	46	Digital IO PAD Default: SCLK of Audio Bus 1 Alternate 1: GPIO3 for internal MCU control Alternate 2: ADV_TIM2 for internal MCU control
AUD1_MCLK	I/O	47	Digital IO PAD Default: MCLK of Audio Bus 1 Alternate 1: GPIO2 for internal MCU control Alternate 2: ADV_TIM1 for internal MCU control
AUD1_D0	I/O	44	Digital IO PAD Default: Data0 of Audio Bus 1 Alternate 1: GPIO0 for internal MCU control Alternate 2: UART_TX for internal MCU control
AUD1_D5	I/O	45	Digital IO PAD Default: Data5 of Audio Bus 1 Alternate 1: GPIO1 for internal MCU control Alternate 2: UART_RX for internal MCU control
AUD2_SCLK	I/O	55	Digital IO PAD Default: SCLK of Audio Bus 2 Alternate 1: GPIO5 for internal MCU control Alternate 2: ADV_TIM2 for internal MCU control
AUD2_MCLK	I/O	56	Digital IO PAD Default: MCLK of Audio Bus 2 Alternate 1: GPIO4 for internal MCU control Alternate 2: ADV_TIM1 for internal MCU control
AUD2_D0	I/O	48	Digital IO PAD Default: Data0 of Audio Bus 2 Alternate 1: GPIO7 for internal MCU control Alternate 2: UART_TX for internal MCU control
AUD2_D1	I/O	49	Digital IO PAD Default: Data1of Audio Bus 2 Alternate 1: GPIO10 for internal MCU control Alternate 2: UART_TX for internal MCU control
AUD2_D2	I/O	50	Digital IO PAD Default: Data2 of Audio Bus 2 Alternate 1: GPIO11 for internal MCU control Alternate 2: UART_RX for internal MCU control

AUD2_D3	I/O	52	Digital IO PAD Default: Data3 of Audio Bus 2 Alternate 1: GPIO12 for internal MCU control Alternate 2: Advanced Timer1 for internal MCU control
AUD2_D4	I/O	53	Digital IO PAD Default: Data4 of Audio Bus 2 Alternate 1: GPIO13 for internal MCU control Alternate 2: Advanced Timer2 for internal MCU control
AUD2_D5	I/O	54	Digital IO PAD Default: Data5 of Audio Bus 2 Alternate 1: GPIO6 for internal MCU control Alternate 2: UART_RX for internal MCU control Alternate 3: CEC
RESETB	I	36	Reset Pin. Low for reset state, High for functional state.
XTALI	I/O	75	25M Crystal Input
XTALO	I/O	76	25M Crystal output
JTAG_TMS	I/O	34	Default: TMS, Internal MCU programming pin Alternate: General Interrupt Output Pin
JTAG_TCK	I	35	Default: TCK, Internal MCU programming pin Alternate: AVMUTE Interrupt Output Pin
EP_SCK	I/O	42	Digital IO PAD Default: EP_SCK for internal MCU SPI control
EP_CSB	I/O	43	Digital IO PAD Default: EP_CSB for internal MCU SPI control
EP_MISO	I/O	39	Digital IO PAD Default: EP_MISO for internal MCU SPI control
EP_MOSI	I/O	40	Digital IO PAD Default: EP_MOSI for internal MCU SPI control
VMON0	I/O	27	VBus0 Monitor Pin
VMON1	I/O	28	VBus1 Monitor Pin
CC0A	I/O	29	Type-C CC0 Pin1
CC0B	I/O	30	Type-C CC0 Pin2
CC1A	I/O	31	Type-C CC1 Pin1
CC1B	I/O	32	Type-C CC1 Pin2
USB_DP	I/O	58	USB 2.0 D+ Pin
USB_DM	I/O	57	USB 2.0 D- Pin

3. Electrical Specifications

3.1 Timing Information

3.1.1 Power Up and Reset Timing Diagrams

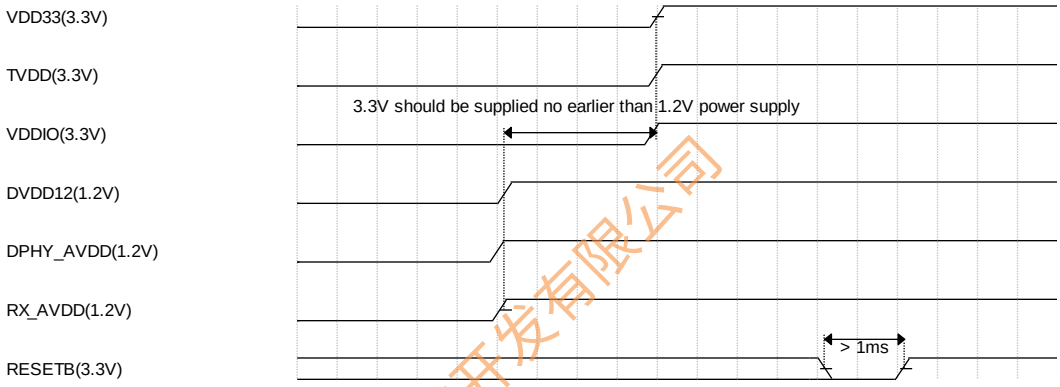


Figure 8. Power Up Sequence

3.1.2 I2C Timing Diagrams

The I2C bus uses 8-bit page address and 16-bit register address. ACK should be provided per 8-bit transaction. For every register, 8-bit data will be accessed. The device address is 0xB0 in 8-bit.

The I2C write timing is shown below.

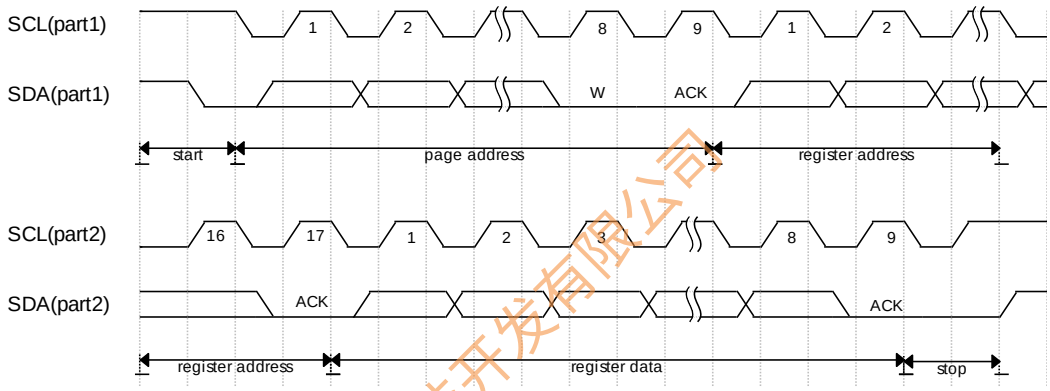


Figure 9. I2C Timing Diagram(Write)

The I2C read timing is shown below.

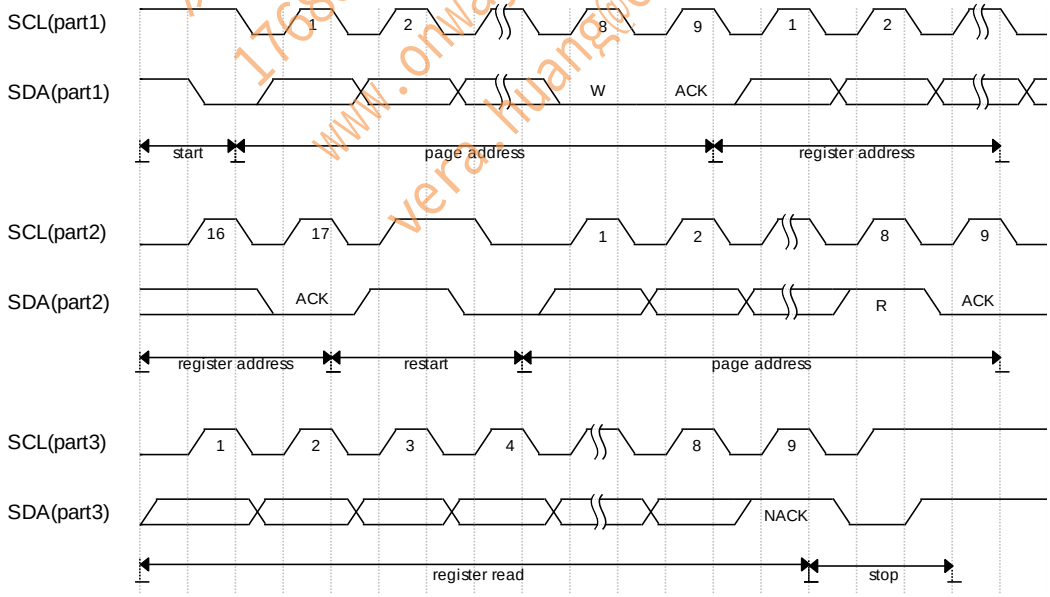


Figure 10. I2C Timing Diagram(Read)

3.2 Operating Conditions

3.2.1 Temperature Conditions

GSV6127EA's operation temperature range is -40 ºC to 85 ºC. The maximum junction temperature is at 125 ºC.

3.2.2 Audio Pin Conditions

GSV6127EA's Audio TTL pin characteristic is the same as other GPIO. By default, Audio pin is TTL push-pull circuit design. Refer to Section 3.2.8 for details.

3.2.3 I2C and SPI Conditions

GSV6127EA's I2C maximum SCL frequency is 400KHz.

Table 6. Recommended SPI Timing Conditions

Symbol	Description	MIN.	TYP.	MAX.	Unit
f_C	Serial Clock Frequency	12.5MHz		25	MHz
t_{CLH}	Serial Clock High Time	18	20	40.11	ns
t_{CKL}	Clock low-level width for QSPI	18	20	38.89	ns
t_{CLCH}	Serial Clock Rise Time	0.2	0.63		V/ns
t_{CHCL}	Serial Clock Fall Time	0.2	0.66		V/ns
t_{SLCH}	CS# Active Setup Time	5	60		ns
t_{CHSH}	CS# Active Hold Time	5	104		ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time (Read/Write)	20	98		ns
t_{CLQX}	Output Hold Time	1.2	1.399		ns
t_{DVCH}	Data In Setup Time	2	17		ns
t_{CHDX}	Data In Hold Time	2	22		ns
t_{HLCH}	HOLD# Low Setup Time (Relative To Clock)	5			ns

t_{HHCH}	HOLD# High Setup Time (Relative To Clock)	5			ns
t_{CHHL}	HOLD# High Hold Time (Relative To Clock)	5			ns
t_{CHHH}	HOLD# Low Hold Time (Relative To Clock)	5			ns
t_{HLQZ}	HOLD# Low To High-Z Output			6	ns
t_{HHQX}	HOLD# High To Low-Z Output			6	ns
t_{CLQV}	Clock Low To Output Valid		4.999	7	ns

Table 7. Recommended I2C Timing Conditions

Symbol	Description	MIN.	TYP.	MAX.	Unit
f_{scl}	Clock Cycle for QSPI		300	400	KHz
t_{LOW}	clock low period	1.3	2		us
t_{HIGH}	clock high period	0.6	0.9		us
t_{BUF}	bus free time before new start	1.3			us
$t_{VD:DAT}$	data valid time			0.9	us
$t_{SU:STO}$	set-up time for stop condition	0.6	0.65		us
$t_{HD:DAT}$	data in hold time	0	1		us
$t_{SU:DAT}$	data in setup time	0.1	0.639		us
t_R	rise time		260	300	ns
t_F	fall time		20	300	ns

3.2.4 Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Digital power supply	DVDD12	-0.3 to 1.4	V
Interface power supply	VDDIO	-0.3 to 4	V
Analog power supply(RX_AVDD,MIPI_AVDD)	AVDD	-0.3 to 1.4	V
Digital IO power supply	VDD33	-0.3 to 4	V
Operating Temperature Range	To	-40 to +85	℃
Storage Temperature Range	Tstg	-40 to +125	℃
Junction Temperature	Tj	+125	℃

3.2.5 ESD Protection

Table 9. ESD Protection

SYMBOL	PARAMETER	VALUE	UNIT
HBM	HBM for SIO(1) pins (JEDEC JS-001-2023)	8000	V
	HBM for other pins (JEDEC JS-001-2023)	4000	V
CDM	ESD CDM (JEDEC JS-002-2022)	1000	V
LU	Latch-up (JED78F)	100	mA

(1) SIO : Include typeC/DP Interface and MIPI interface pins.

3.2.6 Thermal Information

Table 10. Thermal Information

Parameter (1)(2)(3)	Symbol	Value	Unit
Junction-to-ambient thermal resistance	RθJA	19.27	℃/W
Junction-to-board thermal resistance	RθJB	8.54	℃/W
Junction-to-case(top) thermal resistance	RθJCt	3.39	℃/W
Junction-to-case(bottom) thermal resistance	RθJCb	3.53	℃/W
Junction-to-top characterization parameter	ΨJT	0.5	℃/W
Junction-to-board characterization parameter	ΨJB	8.54	℃/W

(1) Test Result according to the JESD51-14 reference document.

(2) PCB Type: JEDEC high-k (2s2p) as defined in JESD 51-7

(3) PCB Size: 76.2mm×114.3mm×1.6mm

3.2.7 Recommended Operating Conditions

Table 11. Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	Unit
Power Pins					
Digital power supply	DVDD12	1.14	1.2	1.26	V
Digital interface IO power supply	VDDIO	3.0	3.3	3.6	V
Analog power supply	AVDD	1.14	1.2	1.26	V
Digital IO power supply	VDD33	3.0	3.3	3.6	V

3.2.8 Electrical Characteristics

Table 12. Electrical Characteristics

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
DisplayPort Receiver Main-Link DC Electrical Characteristics						

Differential Input Termination	Rin		90		110	Ω
Peak-to-Peak Input Differential Swing	VID	VIN+ - VIN-	100		1400	mV
DisplayPort Receiver Main-Link AC Electrical Characteristics						
Unit Interval for HBR3 (8.1Gbps/lane)	UI_HBR3			123		ps
Unit Interval for HBR2 (5.4Gbps/lane)	UI_HBR2			185		ps
Unit Interval for HBR (2.7Gbps/lane)	UI_HBR			370		ps
Unit Interval for RBR (1.62Gbps/lane)	UI_RBR			617		ps
Down Spread Amplitude	SSC	Support frequency rage of 30~33kHZ	0		0.5	%
Jitter Closed-loop Tracking Bandwidth for HBR3	f_{HBR3}		10			MHz
Jitter Closed-loop Tracking Bandwidth for HBR2	f_{HBR2}		10			MHz
Jitter Closed-loop Tracking Bandwidth for HBR	f_{HBR}		10			MHz
Jitter Closed-loop Tracking Bandwidth for RBR	f_{RBR}		5.4			MHz
DisplayPort Receiver AUX DC Electrical Characteristics						
AUX TX Output Differential Peak-to-Peak Voltage	$V_{diff-tx}$		290		1380	mV
AUX RX Output Differential Peak-to-Peak Voltage	$V_{diff-rx}$		270		1360	mV
AUX termination DC resistance	$V_{aux-term}$			100		Ω
Manchester transaction unit interval	UI		0.4		0.6	us
GPIO & Audio						
Input High level	VIH1		0.7*VDD33			V
Input Low level	VIL1				0.3*VDD33	V

Output High level	VOH1	IOH = -4mA	VDD33-0.4			V
Output Low level	VOL1	IOL = 4mA			0.4	V
DisplayPort HPD (Open-Drain Output) need external 1k pull-up resistor to VDD33						
Output Low level	VOL2	IOL = 4mA			0.4	V
I2C Control (Open-Drain)						
Input High level	VIH1		0.7*VDD33			V
Input Low level	VIL1				0.3*VDD33	V
Low level Open-Drain Output Voltage	VOL3	IOL = 4mA			0.4	V
Input Capacitance	CIN				3	pF
VMON Pin						
ADC for VBUS voltage detect	VMON		0.4		2	V
ResetB Pin						
Chip Reset(Active low) Voltage	VIH-rstb		2.5		VDD33+ 0.3	V
	VIL-rstb		-0.3		0.9	

3.2.9 Electrical Characteristics for Parallel Bus

Table 13. Electrical Characteristics for Parallel Bus

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
MIPI DPHY LP Transmitter DC Electrical Characteristics						
LP output high level output voltage	VOH		0.95	1.2	1.3	V
LP output low level output voltage	VOL		-50		50	mV
Output impedance	ZOLP		110			Ω
MIPI DPHY HS Transmitter DC Electrical Characteristics						
HS transmit static common-mode voltage	VCMTX	ZID = 100Ω	150	220	250	mV
VCMTX Mismatch when Output is differential-1 or differential-0	|△VCMTX(1,0)|	ZID = 100Ω			5	mV
HS transmit differential voltage	|VOD|	ZID = 100Ω	140	180	270	mV
VOD Mismatch when Output is differential-1 or differential-0	|△VOD|	ZID = 100Ω			14	mV
HS output high voltage	VOHHS	ZID = 100Ω			360	mV
Single-ended output impedance	ZOS		40	50	60	Ω

Single-ended output impedance mismatch	$\triangle$ZOS			10		%
MIPI DPHY LP Transmitter AC Electrical Characteristics						
15% to 85% rise time and fall time	t_{RLP}/t_{FLP}				25	ns
30% to 85% rise time and fall time	t_{REOT}	0-60pF at RX term center tap			35	ns
Load capacitance	C_{LOAD}				70	pF
MIPI DPHY HS Transmitter AC Electrical Characteristics						
Common level variations, HF	$\triangle V_{CMTX}(HF)$	> 450MHz			15	mV_{RMS}
Common level variations, LF	$\triangle V_{CMTX}(LF)$	50MHz to 450MHz			25	mV_{PEAK}
20% to 80% rise time and fall time	t_R and t_F	<1Gbps			0.3	UI
			150			ps
		1 Gbps ~1.5 Gbps			0.35	UI
			100			ps
		>1.5Gbps			0.4	UI
			50			ps
Data lane bit rate	DLBR		80		2500	Mbps
Clock lane frequency	CL_{FREQ}		40		1250	MHz
MIPI DPHY DATA-CLOCK TIMING						
UI instantaneous	UI_{INST}		0.4		12.5	ns
Data to clock skew	t_{SKEW}	80M~ 1.0Gbps	-0.15		0.15	UI_{INST}
		1.0 Gbps~ 1.5Gbps	-0.2		0.2	
Static data to clock skew	t_{SKEW} Static	> 1.5Gbps	-0.2		0.2	UI_{INST}
Dynamic data to clock skew	t_{SKEW} Dynamic	> 1.5Gbps	-0.15		0.15	UI_{INST}

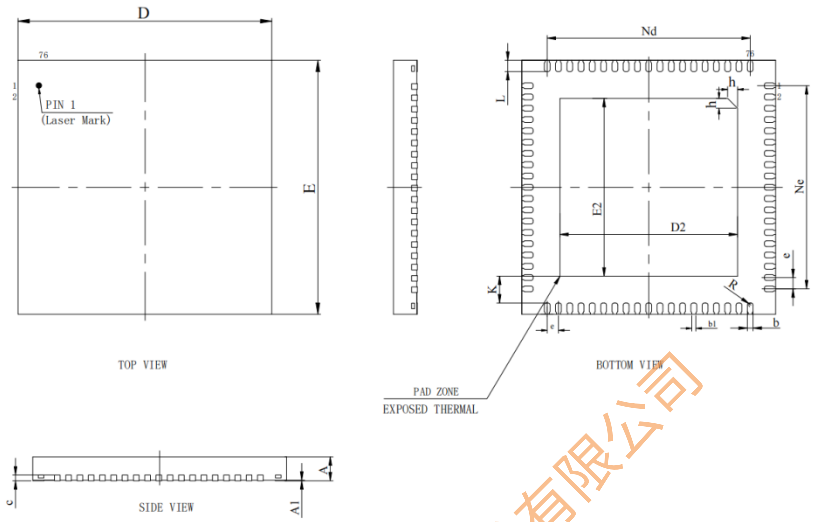
3.2.10 Power Consumption

Tested under condition: VDD33=VDDIO=3.3V, RX_AVDD=1.2V, MIPI_AVDD=1.2V, DVDD12=1.2V, Temp=25℃.

Table 14. Power Information

Resolution	Test Condition	VDD33 &VDDIO	AVDD	DVDD12
3840*2160@60Hz	DP-4lane*5.4Gbps With HDCP2.3 to MIPI-4laneCSI D-PHY	37mA	500mA	218mA
3840*2160@30Hz	DP-4lane*2.7Gbps With HDCP2.3 to MIPI-4lane CSI D-PHY	37mA	440mA	146mA
1920*1080@60Hz	DP-4lane*1.62Gbps With HDCP2.3 to MIPI-4lane CSI D-PHY	30mA	400mA	108mA

4. Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
● A	0.80	0.85	0.90
● A1	0.00	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.203REF		
● D	8.90	9.00	9.10
D2	6.20	6.30	6.40
e	0.40BSC		
Nd	7.20BSC		
● E	8.90	9.00	9.10
E2	6.20	6.30	6.40
Ne	7.20BSC		
L	0.35	0.40	0.45
K	0.95REF		
R	0.075REF		
h	0.30	0.35	0.40

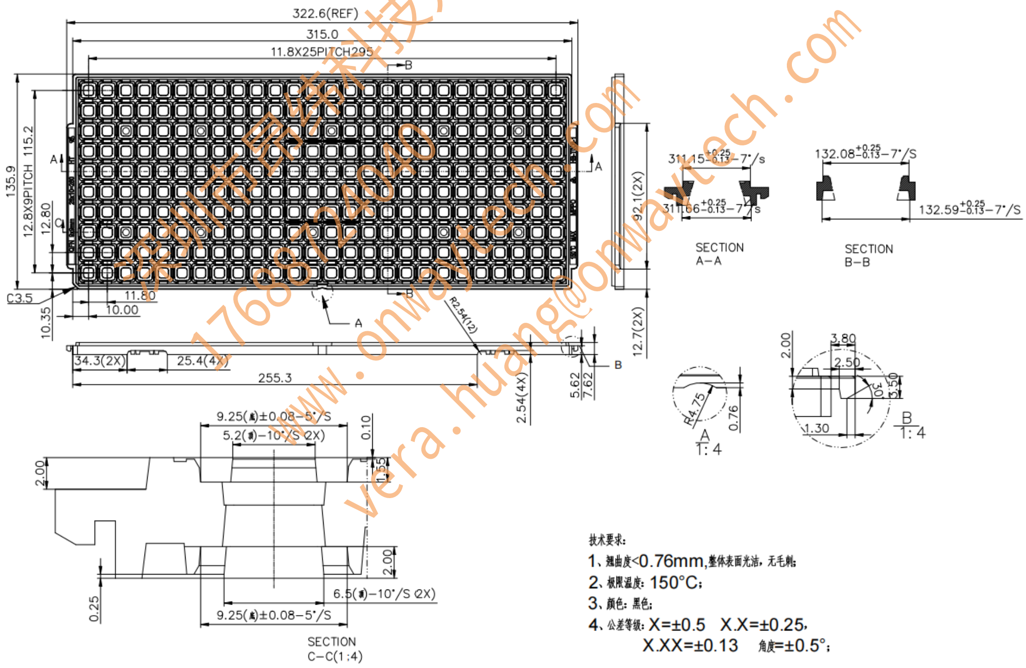


Figure 11. Package Dimensions (QFN76)

5. Ordering Guide

Table 15. Ordering Information

Part Number.	Temperature Range	Package Description	Packing Type
GSV6127E	−40°C to +85°C	QFN76	Tray

6. Revision History

Table 16. Revision history

Revision No.	Description	Date
V0.1	Draft Initial Version for internal review.	Oct 21, 2022
V0.2	Correct function description	Jun 8, 2023
V0.3	Correct Pin Description	July 12, 2023
V0.4	Update Pin definition for mass production application	Aug 10, 2023
V0.5	Modify Pin17/18 to GPIO function	Nov 13,2023
V0.6	Add C-PHY description, Remove eDP description	Dec 1, 2023
V0.7	Update block diagrams on flash description	Jan 17, 2024
V0.8	Add description of CP	Apr 13, 2024
V0.9	Pin Mapping Update, Remove C-PHY description	May 5, 2024
V0.10	Typo Fix and add back HDMI 2.0 Rx support	Jun 27, 2024
V0.11	Merge Characteristic Information into datasheet	Jul 2, 2024
V0.12	Remove SPI feature support from pin description	Sep 8, 2024
V0.13	Update I2C/SPI and I2S timing information	Dec 18, 2024
V0.14	Remove TTL description	Dec 19, 2024
V0.15	Add VESA LVDS Pin description	Apr 9, 2025
V0.16	Modify latch-up data	Jun 10, 2025
V0.17	Correct HDMI TMDS polarity to match schematic	Jul 4, 2025
V1.0	Remove “Preliminary”, TVDD/DPHY_AVDD Pin renamed	Jul 7, 2025

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